Sub Code: R2331022 **R23** **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURUJADA VIZINAGARAM
III B. Tech I Semester Regular Examinations November -2025
DIGITAL CIRCUITS
(DEPARTMENT OF EEE)

Time: 3 hours **Max. Marks: 70**

The Question paper consists of Part A & Part B.
Part A is compulsory, Answer all questions. Part B Answers any one question from each unit.
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1		PART-A	(20Marks)
	a)	What are don't care terms?	[2]
	b)	State the concept of parallel binary adder	[2]
	c)	What are the draw backs of PLAs	[2]
	d)	Implement a 4×1 mux using 2×1 mux's	[2]
	e)	What are the differences between combinational and sequential logic circuits?	[2]
	f)	List the applications of shift registers	[2]
	g)	What is the need of state reduction in sequential circuit design?	[2]
	h)	What is finite state Machine?	[2]
	i)	Define propagation delay time.	[2]
	j)	Define fan-in, fan-out	[2]
		PART-B	(50Marks)
		Question from **Unit - I**	
2	a)	Simplify the following function using K-Map method $F(A,B,C,D)= \Sigma m(0,1,2,3,4,6,9,10)+d(7,11,12,13,15)$	[5]
	b)	Design a 2-bit comparator using gates	[5]
		(OR)	
3	a)	Implement Boolean expression for EX-OR gate using NAND gates	[5]
	b)	minimize the expression using Quine Mc-cluskey method $Y= \Sigma m(2,4,5,9,12,13)$	[5]
		Question from **Unit - II**	
4	a)	Draw the logic diagram of a 2 line to 4 line decoder	[4]
	b)	Implement the following Boolean function using 4:1 MUX .$F(A,B,C,D)=\sum m(0,1,2,4,6,9,12,14)$	[6]
		(OR)	
5	a)	Design a 4 input priority encoder.	[5]
	b)	Implement $F = \sum m(2,3,4,5,7)$ using PAL.	[5]
		Question from **Unit - III**	
6	a)	Convert a clocked S-R flip flop to a T-flip flop.	[5]
	b)	Design a mod-11 asynchronous counter using T flip flops and discuss its disadvantages.	[5]
		(OR)	
7	a)	Draw the schematic circuit of J-K flip-flop and explain its operation with the help of truth table.	[5]
	b)	Distinguish between Synchronous & asynchronous counters.	[5]
		Question from **Unit - IV**	
8	a)	Explain the different methods of state assignment.	[5]
	b)	Compare Mealy and Moore machines	[5]
		(OR)	
9	a)	Explain the steps involved in the design of asynchronous	[5]

		sequential circuit	
	b)	Discuss about completely and incompletely specified sequential machines.	[5]
		Question from **Unit - V**	
10	a)	What is logic family. Give the classification of logic family	[5]
	b)	Draw and explain the circuit diagram of two-input TTL NAND gate. what are the advantages and disadvantages of this logic family .	[5]
		(OR)	
11	a)	Discuss CMOS NAND gate .what are advantages of CMOS logic	[5]
	b)	Discuss emitter coupled logic .	[5]

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